

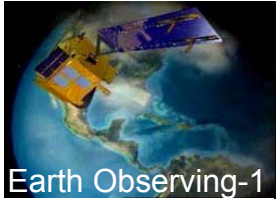
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Section 24

Wideband Advanced Recorder Processor (WARP)

. . . Terry Smith

*Flight Electronics Branch, Electric Systems Center
NASA Goddard Space Flight Center*

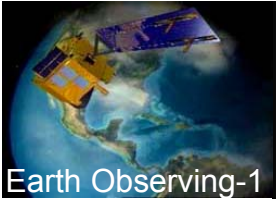


Overview



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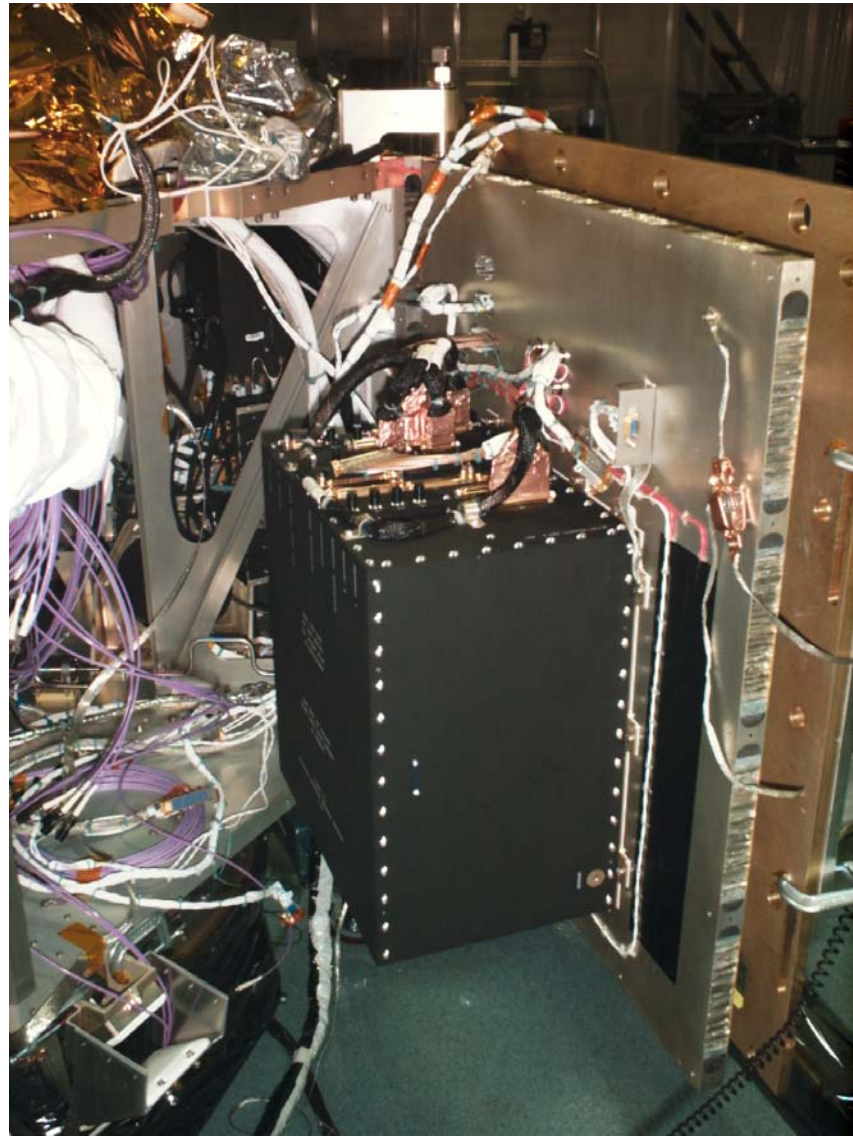
- ◆ ***The WARP is a spacecraft component that receives, stores, and processes high rate science data and its associated ancillary data from multispectral detectors, hyperspectral detectors, and an atmospheric corrector, and then transmits the data via an X-band or S-band transmitter to the ground station.***
- ◆ ***WARP Goals***
 - *Pathfinder for next generation LANDSAT mission.*
 - *Flight prove architectures and technologies.*
 - *Identify future technology needs.*

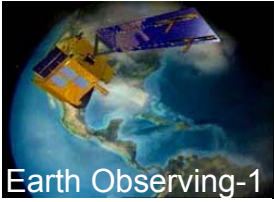


WARP on Spacecraft Bay 1



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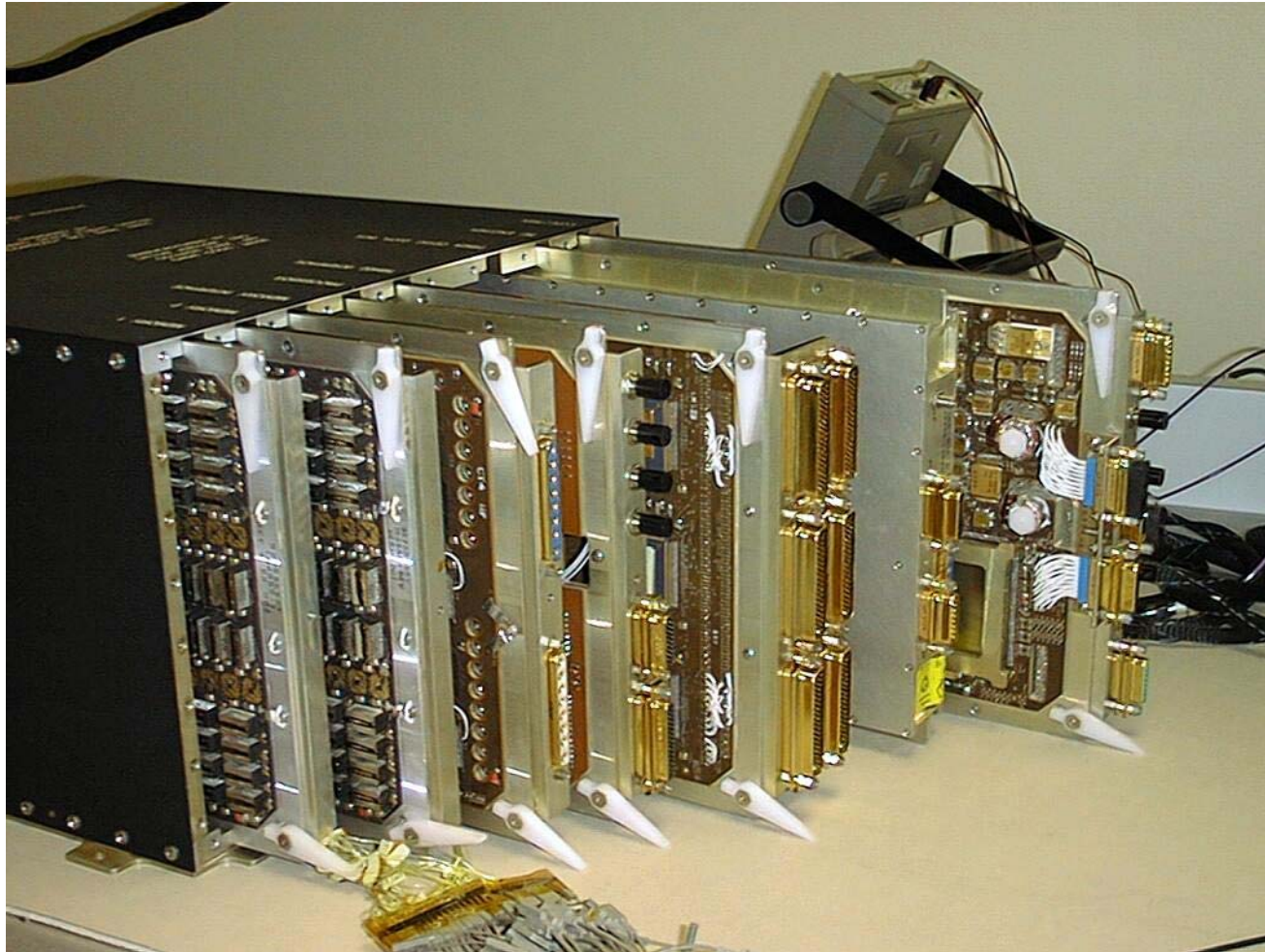


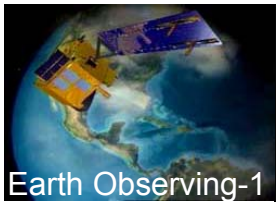


Circuit Card Assemblies



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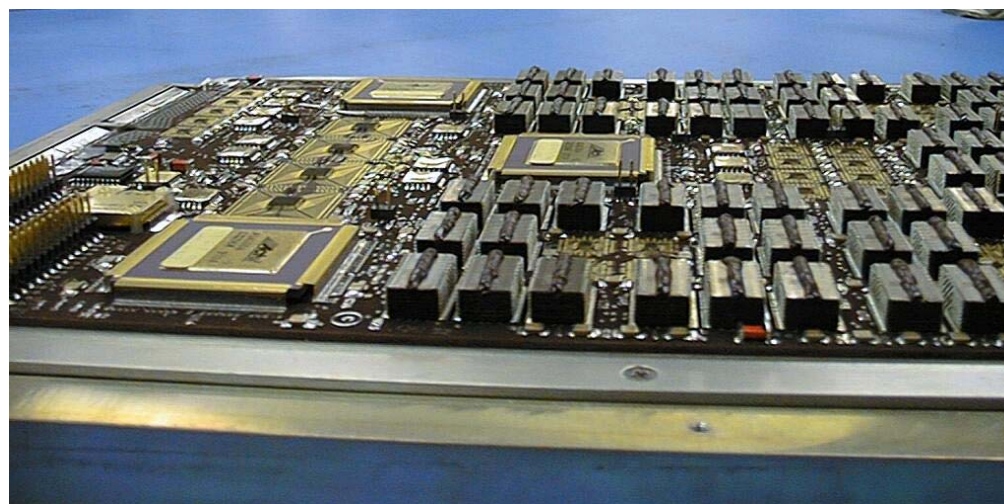
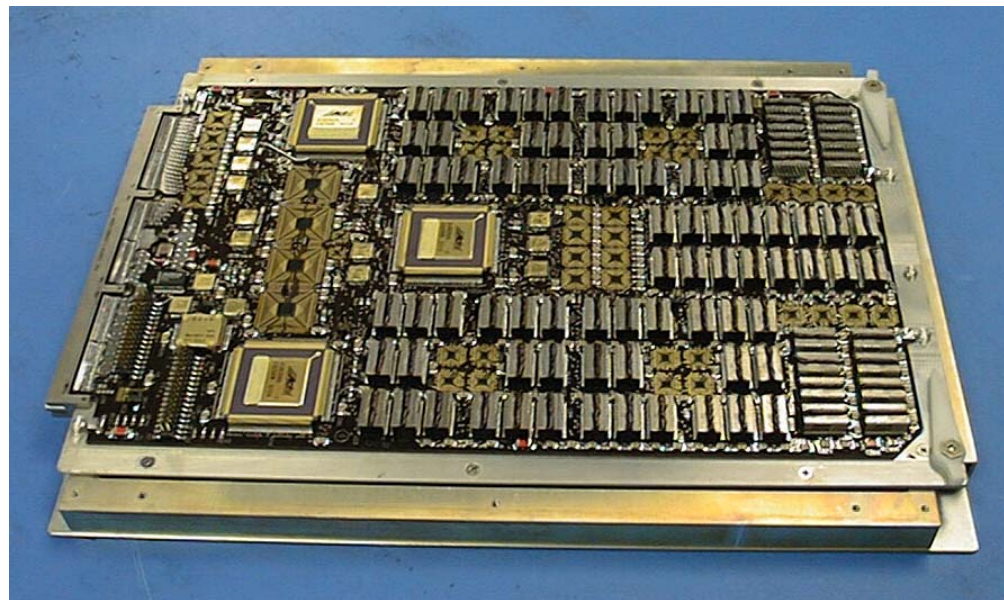
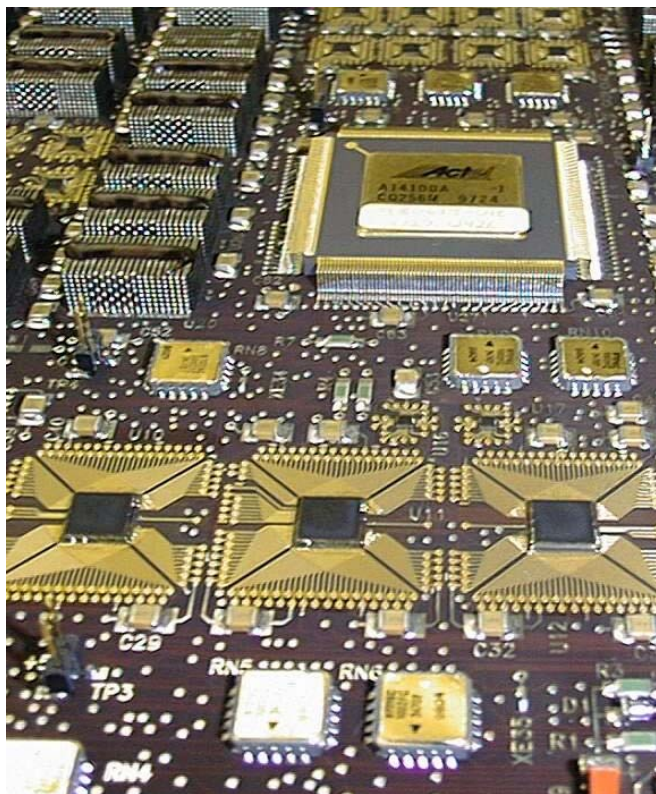


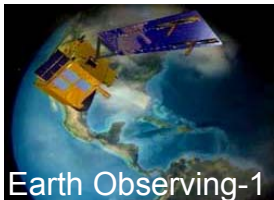


Memory Board



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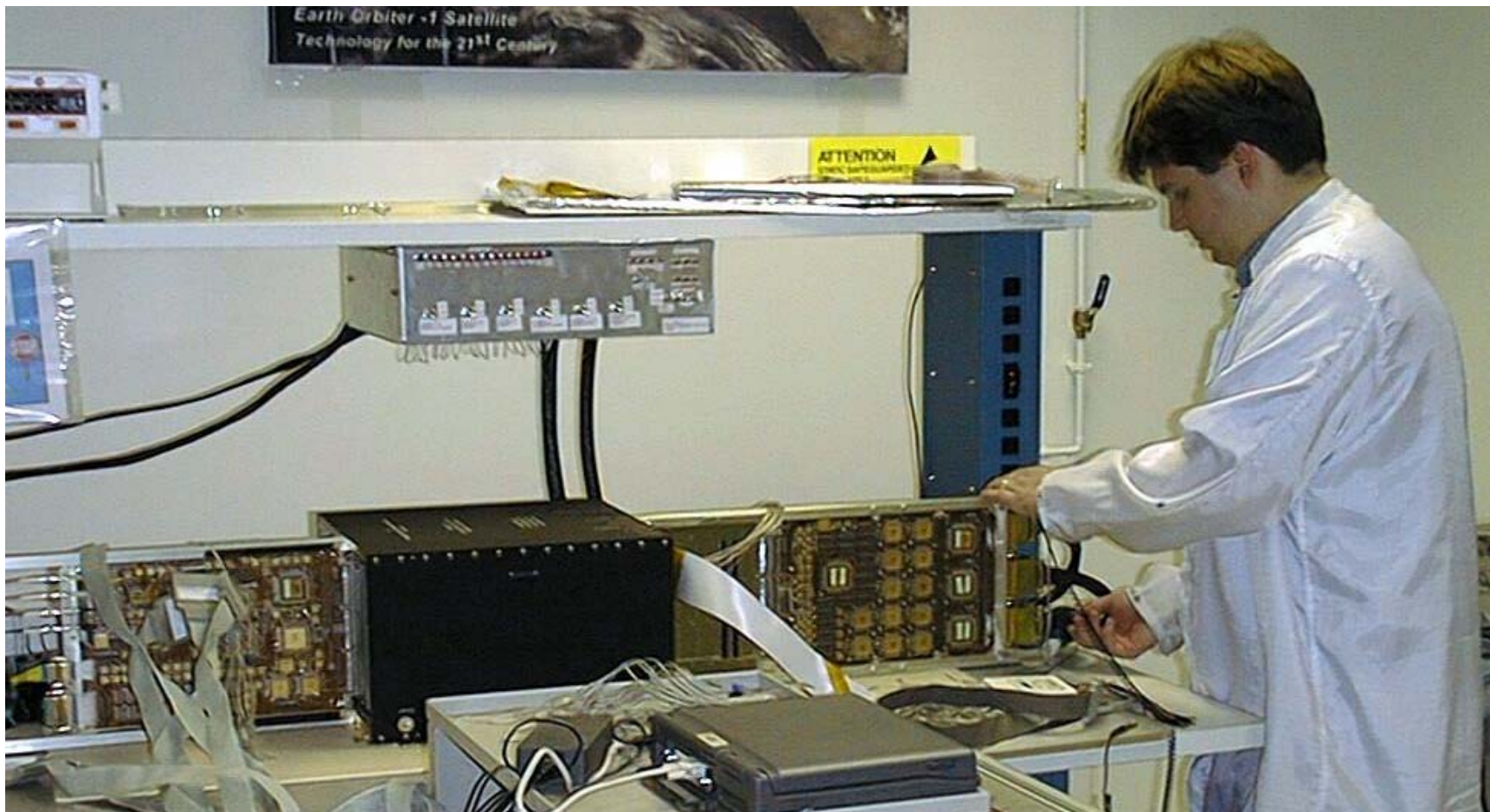


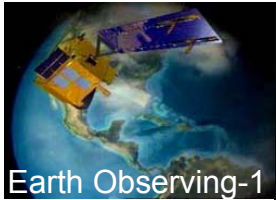


Integration & Test



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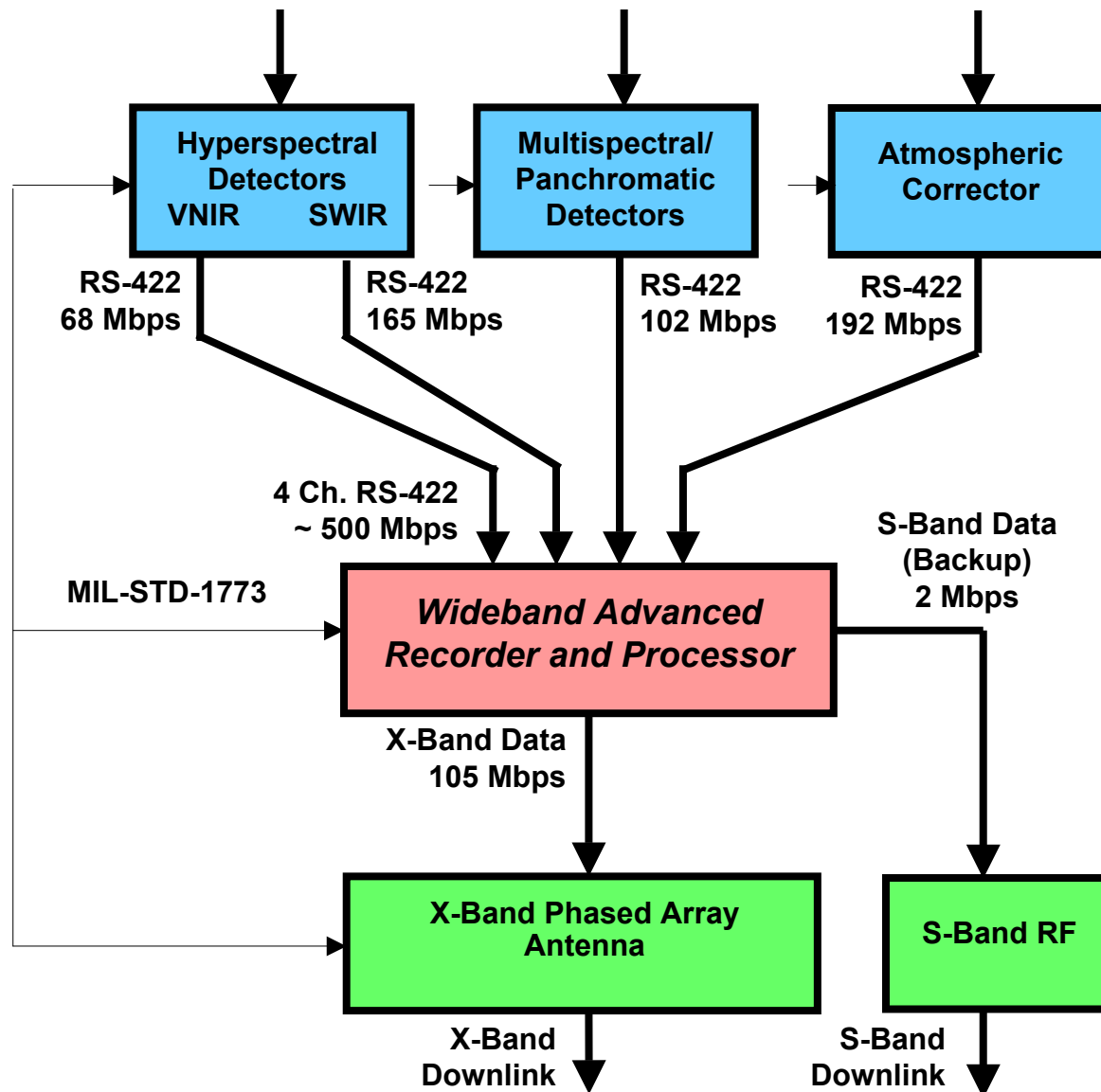


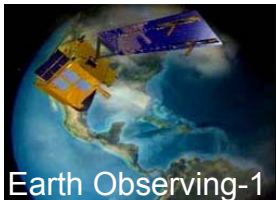
Earth Observing-1

Spacecraft Data System Architecture



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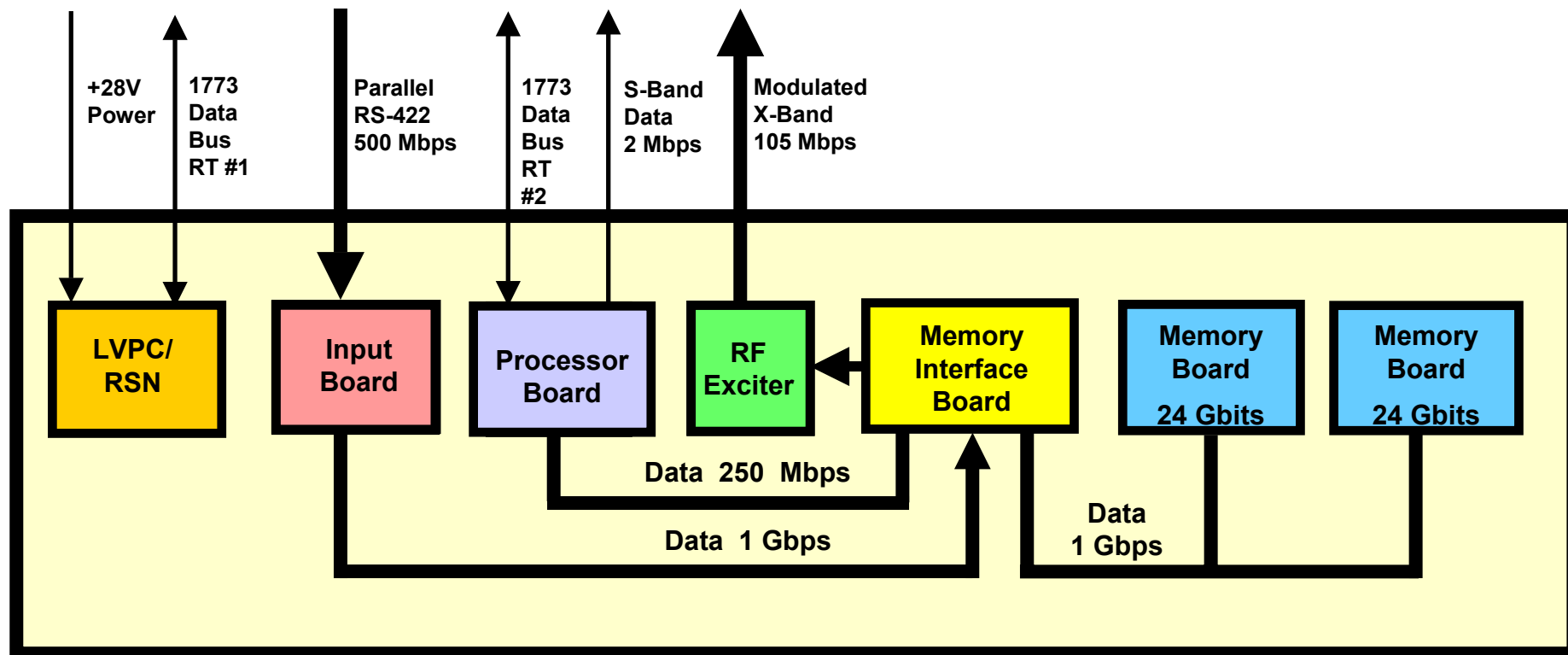


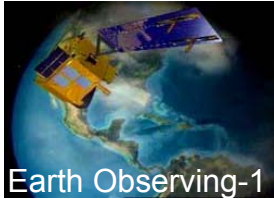
Earth Observing-1

Hardware Architecture



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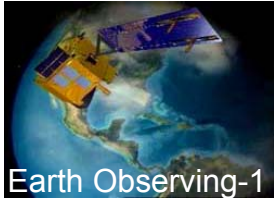


WARP Specifications



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| | |
|-----------------------------------|--|
| <i>Data Storage:</i> | <i>48 Gbits</i> |
| <i>Data Record Rate:</i> | <i>900 Mbps</i> |
| <i>Data Playback Rate:</i> | <i>105 Mbps (with built-in X-Band RF modulator)</i> |
| <i>Data Processing:</i> | <i>Post-Record Data Processing Capability</i> |
| <i>Size:</i> | <i>25 x 39 x 37 cm</i> |
| <i>Mass:</i> | <i>18 kg</i> |
| <i>Power:</i> | <i>38 W Orbital Average, 87 W Peak</i> |
| <i>Thermal:</i> | <i>0-40° C Minimum Operating Range</i> |
| <i>Mission Life:</i> | <i>1 Year Minimum</i> |
| <i>Radiation :</i> | <i>15 krad total dose, LET 35 MeV</i> |

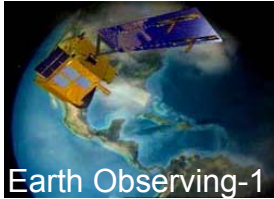


Operational Performance



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- ◆ **Over 2,500 record and playback operations**
- ◆ **One anomaly since launch (on June 22, 2001)**
 - **Uncorrectable data errors out of Memory Board #2 (outermost board)**
 - **Most likely caused by single-event-upset in Memory Board FPGA**
 - **Reset of Memory Board cured the anomaly**



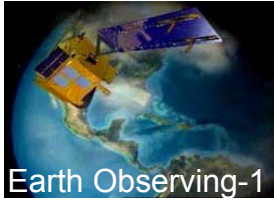
Critical Technologies

(Mongoose 5 Microprocessor)



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- ◆ ***Technology Description***
 - *Rad-Hard, 32 bit, 12 MHz Microprocessor*
 - *MIPS R3000 Instruction Set*
 - *MIPS R3010 Floating-Point Unit*
 - *6 kbyte on-chip memory cache*
- ◆ ***Technology Validation***
 - *Flawless Operation*
 - *Data Processing Software not yet implemented*
- ◆ ***Technology Usage***
 - *Primary controller of WARP operation*
 - *Post-Record Data Processing Capability*
- ◆ ***Technology Transfer***
 - *Available to industry by Synova*

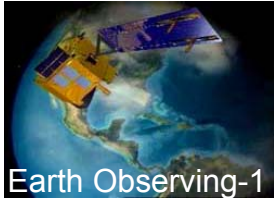


Critical Technologies *(Essential Services Node)*



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- ◆ ***Technology Description***
 - *Remote C&DH Multi-Chip Module*
 - *UTMC UT69R000 16-bit microprocessor*
 - *MIL-STD-1553 Data Bus RT Interface*
 - *Digital and Analog Interfaces*
- ◆ ***Technology Validation***
 - *Flawless Operation*
- ◆ ***Technology Usage***
 - *Subsystem Remote Interface*
 - *Command and Telemetry Functions*
 - *Power Switching Control*
- ◆ ***Technology Transfer***
 - *No Longer Manufactured*

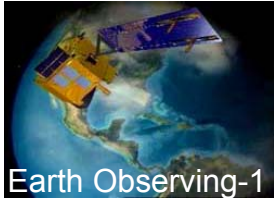


Critical Technologies (EDAC/HS Encoder/Decoder)



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- ◆ **Technology Description**
 - *Error Detection & Correction Chip*
 - *Reed-Solomon Encoder/Decoder*
 - *500 Mbytes per second*
 - *Total Dose 1 x 10E6 Rads*
- ◆ **Technology Validation**
 - *First Flight*
 - *Flawless Operation*
- ◆ **Technology Usage**
 - *Bulk DRAM Error Handling*
- ◆ **Technology Transfer**
 - *Honeywell CMOS Gate Array HX2160*
 - *University of New Mexico: 505-272-7040*



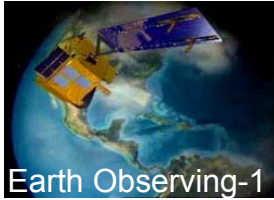
Critical Technologies

(USES Data Compression Chip)



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- ◆ ***Technology Description***
 - *Rad-Hard Lossless Data Compression Chip*
 - *Rice Algorithm*
 - *20 M samples/second*
 - *1.8:1 Typical Compression Ratio*
- ◆ ***Technology Validation***
 - *Control software not yet implemented*
 - *Entropy-Reduction S/W not implemented*
- ◆ ***Technology Usage***
 - *Optional Science-Data Compression*
- ◆ ***Technology Transfer***
 - *Already Flown on Many Missions*
 - *University of New Mexico: 505-272-7040*

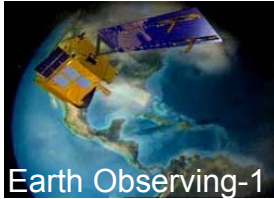


Critical Technologies (Actel 14100 FPGA)



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- ◆ **Technology Description**
 - *Field Programmable Gate Array*
 - *15,000 Gates*
 - *60 Mhz operation*
 - *Single-Event-Upset LET = 5 Mev*
- ◆ **Technology Validation**
 - *15 14100 FPGAs used in WARP*
 - *1 single-event-upset over 7 months*
- ◆ **Technology Usage**
 - *General Purpose Logic Device. Examples:*
 - *CCSDS formatting*
 - *Memory Controller*
 - *Data Bus Interface Controller*
- ◆ **Technology Transfer**
 - *Available to industry by Actel*
 - *Part #: 5962-9552102MYC*



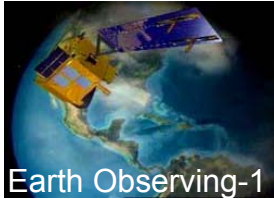
Critical Technologies

(16 Mbit DRAM in 8 High Stack)



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- ◆ **Technology Description**
 - *Dynamic Random Access Memory*
 - *16 Mbit, 4 Mbit x 4, plastic parts*
 - *Low Power CMOS*
 - *4×10^{-6} upset/bit/day*
- ◆ **Technology Validation**
 - *Numerous Single-Bit Flips in normal ops*
 - *All correctable thus far into mission*
- ◆ **Technology Usage**
 - *Processor Board RAM for Code and Data Bulk Memory Boards*
- ◆ **Technology Transfer**
 - *Samsung 16 Mbit DRAM no longer available*
 - *New Designs now using 64 Mbit DRAM*
 - *Stacking available from Vertical Circuits*



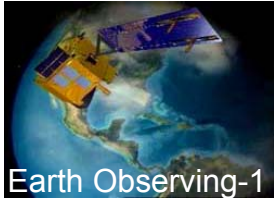
Critical Technologies

(First In First Out (FIFO) Parts)



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- ◆ **Technology Description**
 - *Rad-Hard CMOS FIFOs*
 - *1k x 36 bit and 4k x 9 bit parts*
 - *17 ns access time*
 - *1 Mrad total dose, 1x10E-10 SEU /bit/day*
- ◆ **Technology Validation**
 - *Flawless Operation on orbit*
 - *1 Design Flaw*
- ◆ **Technology Usage**
 - *Science Data Input Buffers*
 - *Backplane Data Bus, Data Rate Buffers*
 - *Playback Data Rate Buffers*
- ◆ **Technology Transfer**
 - *Available to industry by BAE Systems*
 - *866-530-8104 (x4754)*



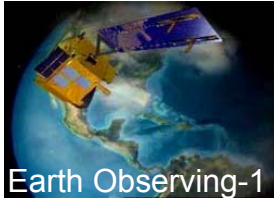
Critical Technologies

(Chip On Board Packaging)



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- ◆ ***Technology Description***
 - *Original Goal was Flip-Chip technology*
 - *Back-Up was wire-bond technology*
 - *Die adhered directly to board*
- ◆ ***Technology Validation***
 - *Flawless Operation on-orbit*
 - *Severe handling constraints and risk*
 - *Time Consuming Manufacturing*
 - *Quality Assurance Concerns*
- ◆ ***Technology Usage***
 - *Memory Board Logic*
 - *Significant Increase in Packaging Density*
- ◆ ***Technology Transfer***
 - *Wire-Bonding to boards not recommended*



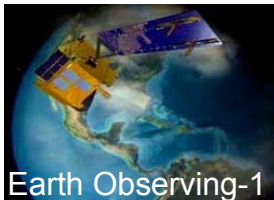
Critical Technologies

(Science Data Processing Software)



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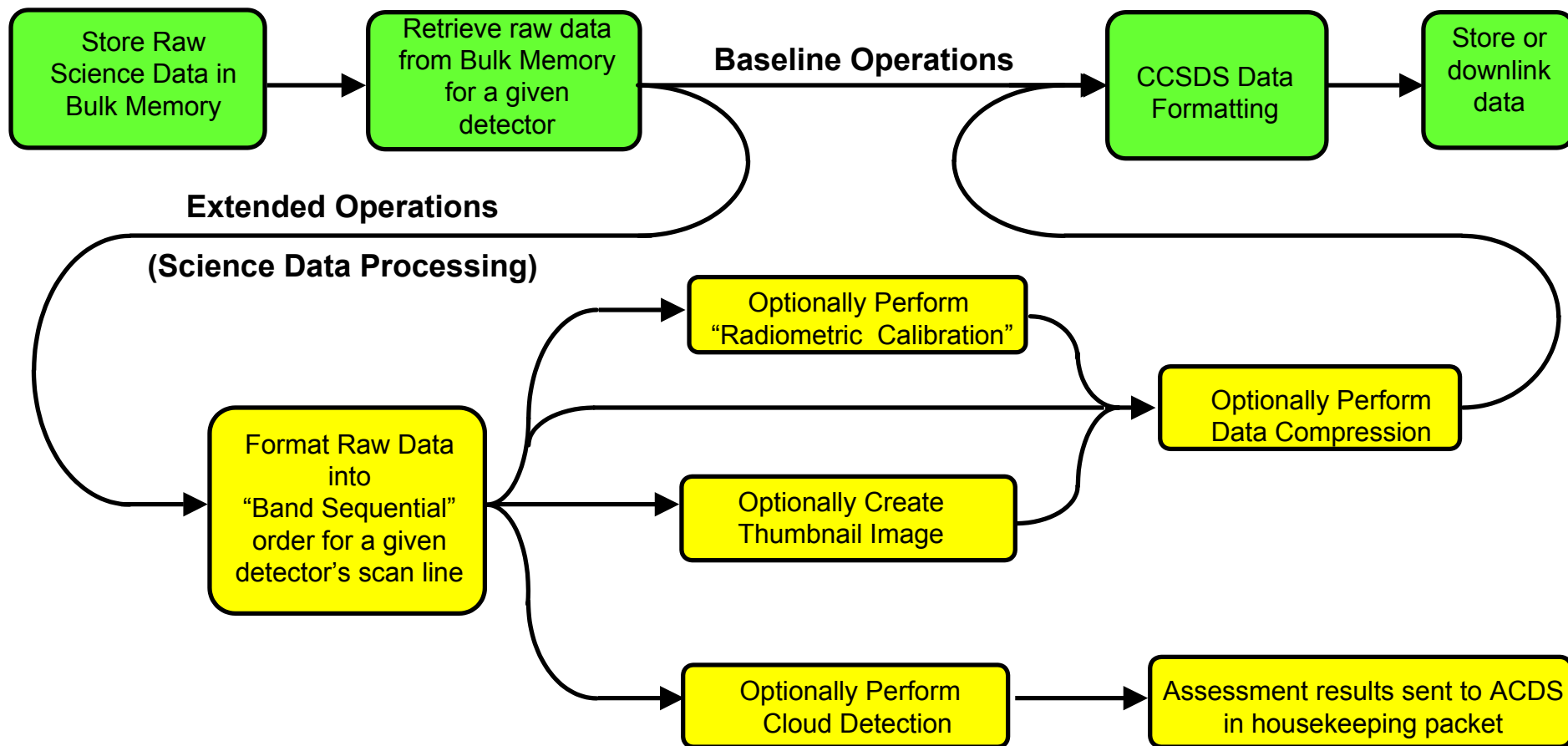
- ◆ ***Technology Description***
 - *Band-Sequential Data Ordering*
 - *Thumbnail Imaging*
 - *Cloud Detection*
- ◆ ***Technology Validation***
 - *To Be Determined*
- ◆ ***Technology Usage***
 - *Entropy Reduction for Data Compression*
 - *Operations Flexibility Demonstration*
- ◆ ***Technology Transfer***
 - *To Be Determined*

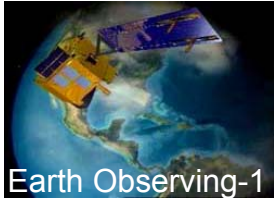


Science Data Processing Software



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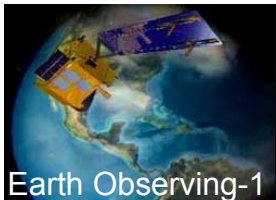
Industry Solid State Recorder Technology



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SEAKR QuickBird, JPL/Ball QuickScat 6/99

| | |
|---------------------------------|--|
| <i>Data Storage:</i> | <i>618 Gbits</i> |
| <i>Data Record Rate:</i> | <i>6 channels @ 800 Mbps each</i> |
| <i>Size:</i> | <i>2 boxes, each 25x51x28 cm</i> |
| <i>Mass:</i> | <i>2 boxes, each 41 kg</i> |
| <i>Power:</i> | <i>240 W</i> |
| <i>Thermal:</i> | <i>0-40 °C</i> |
| <i>Redundancy:</i> | <i>LVPC and Control Cards</i> |
| <i>Radiation :</i> | <i>40 krad total dose, LET 80 MeV</i> |

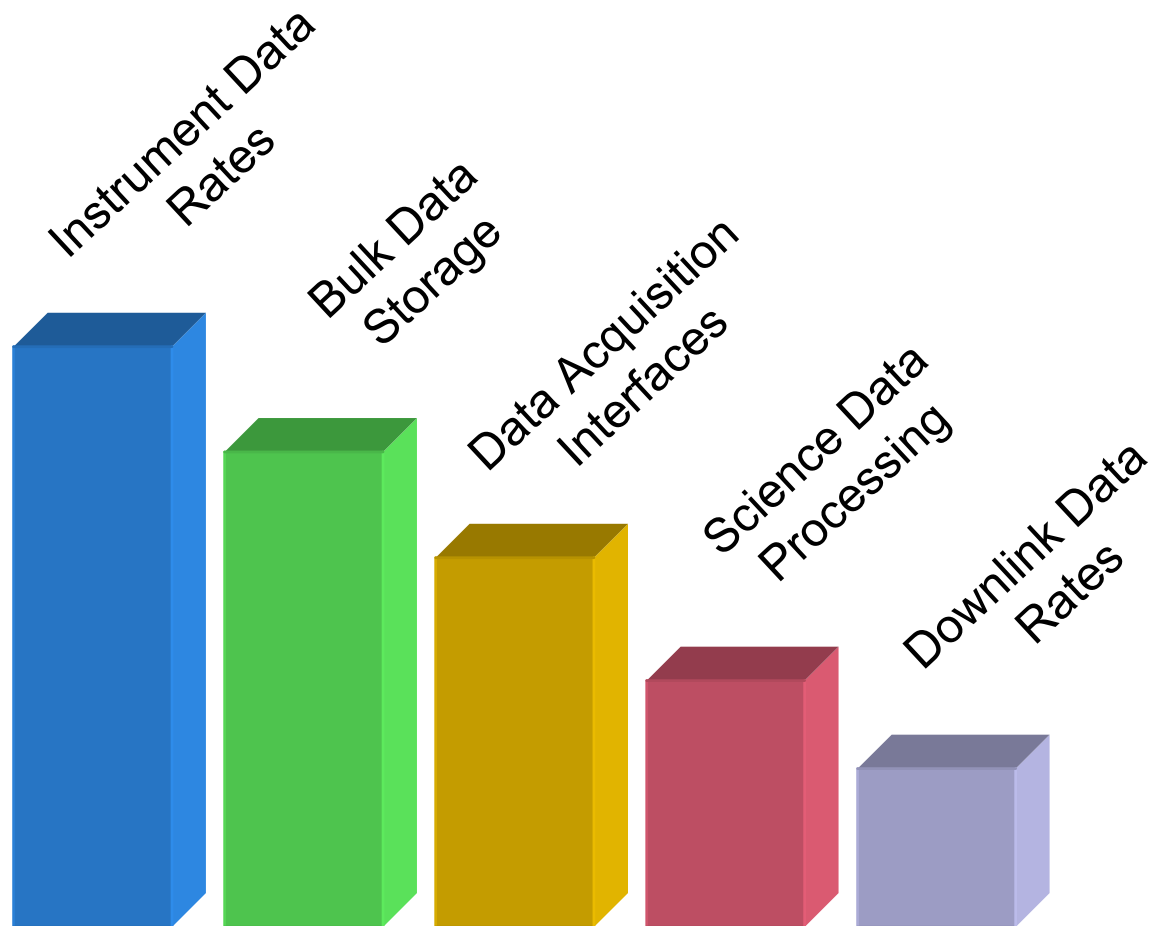


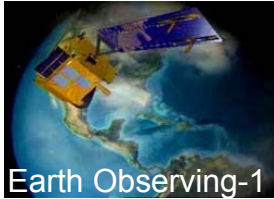
Technology Trends



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*Relative
Advancement
in Technology*



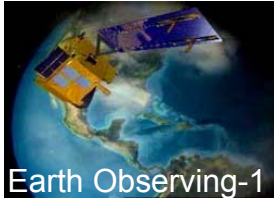


Technology Priorities



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- ◆ **Bulk Data Storage**
 - *256 Mbit Rad-Hard DRAM*
- ◆ **Data Acquisition Interfaces**
 - *High Rate Data Busses*
 - *High Rate, Point-To-Point Data Interfaces*
- ◆ **Other Data Interfaces**
 - *Ethernet I&T Interface*
 - *Standard High Rate Backplane Data Bus*
- ◆ **Science Data Processing**
 - *Re-Configurable Array Processors*
 - *High Performance Data Compression*
- ◆ **Downlink Data Rates**
 - *KA Band or Optical Downlink*
 - *8 Phase Shift Keying (8PSK) Downlink*

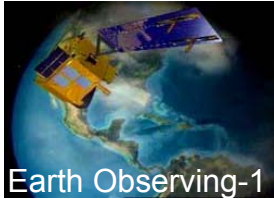


Lessons Learned



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- ◆ ***Engineering Test Units are Essential. Omission results in reliability risks and schedule delays.***
- ◆ ***Don't Use Wire-Bonding on Boards***
- ◆ ***Power-Up of Memory Boards must be staggered***
- ◆ ***Rear Backplane Connectors were very valuable***
- ◆ ***Use CRC code in the downlink data format for real-time data quality checking***
- ◆ ***Provide external box connector for I&T primary power input***



Summary / Conclusions



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- 1) High Performance Data Compression (nearly lossless) is essential if the science community demands full spatial coverage, wide spectral coverage, high pixel resolution raw data. Otherwise, the size, mass, and power will be prohibitive.***
- 2) New technologies must be developed prior to flight projects (IR&D mode) to avoid schedule delays.***
- 3) The flight data systems that are required to handle extremely high data rates require significant development time. Therefore, their development should begin early, when the instrument development begins.***